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PAN1322-SPP

Intel's
BlueMoonUniversal Platform

Wireless Modules

User's Manual

Hardware Description
Revision 1.2

Panasonic

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Rev1.1	Delete chapter 4.3, Update module picture on page 8, delete antenna reference list in chapter 9.1, update chapter 9.8
Rev1.2	Refer in chapter 1.7 FW Version to Appendix [2]

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Table of Contents

Table of Contents . . . 4
List of Figures . . . 6
List of Tables . . . 7
1 General Device Overview . . . 8
1.1 Features . . . 8
1.2 Block Diagram . . . 9
1.3 Pin Configuration LGA . . . 9
1.4 Pin Description . . . 10
1.5 System Integration . . . 13
1.6 SW Patch in EEPROM . . . 14
1.7 FW Version . . . 14
2 Basic Operating Information . . . 15
2.1 Power Supply . . . 15
2.2 Clocking . . . 15
2.3 Low Power Modes . . . 15
2.3.1 Low Power Mode . . . 15
2.3.2 Complete Power Down . . . 15
2.3.3 ON/OFF . . . 15
3 PAN1322-SPP Interfaces . . . 16
3.1 UART Interface . . . 16
3.1.1 UART . . . 16
3.1.1.1 Baud Rates . . . 16
3.1.1.2 Detailed UART Behavior . . . 17
3.1.1.3 UARTCTS Response Time . . . 17
3.2 Low Power Control . . . 17
4 General Device Capabilities . . . 18
4.1 RF Test Application . . . 18
4.2 Firmware ROM Patching . . . 18
4.2.1 Patch Support . . . 18
5 Ordering Information . . . 18
6 Bluetooth Capabilities . . . 19
6.1 Supported Features . . . 19
6.2 PAN1322-SPP Bluetooth Features . . . 19
6.2.1 Secure Simple Pairing . . . 19
6.2.2 Role Switch . . . 19
6.2.3 Sniff Mode . . . 19
6.2.4 Sniff Subrating . . . 19
6.2.5 Enhanced Power Control . . . 19
6.2.6 Encryption Pause and Resume . . . 20
7 Electrical Characteristics . . . 21
7.1 Absolute Maximum Ratings . . . 21
7.2 Operating Conditions . . . 21
7.3 DC Characteristics . . . 22
7.3.1 Pad Driver and Input Stages . . . 22
7.3.2 Pull-ups and Pull-downs . . . 24

7.3.3 Protection Circuits . . . 24
7.3.4 System Power Consumption . . . 25
7.4 RF Part . . . 25
7.4.1 Characteristics RF Part . . . 25
7.4.1.1 Bluetooth Related Specifications . . . 25

8 Package Information . . . 29
8.1 Package Marking . . . 29
8.2 Production Package . . . 29
8.2.1 Pin Mark . . . 30

9 Bluetooth Qualification and Regulatory Certification . . . 31
9.1 Reference Design . . . 31
9.2 FCC Class B Digital Devices Regulatory Notice . . . 32
9.3 FCC Wireless Notice . . . 32
9.4 FCC Interference Statement . . . 33
9.5 FCC Identifier . . . 34
9.6 European R&TTE Declaration of Conformity . . . 34
9.7 Bluetooth Qualified Design ID . . . 36
9.8 Industry Canada Certification . . . 36
9.9 Label Design of the Host Product . . . 36
9.10 Regulatory Test House . . . 36

10 Assembly Guidelines . . . 37
10.1 General Description of the Module . . . 37
10.2 Printed Circuit Board Design . . . 37
10.3 Solder Paste Printing . . . 39
10.4 Assembly . . . 39
10.4.1 Component Placement . . . 39
10.4.2 Pin Mark . . . 39
10.4.3 Package . . . 40
10.5 Soldering Profile . . . 41
10.6 Rework . . . 42
10.6.1 Removal Procedure . . . 42
10.6.2 Replacement Procedure . . . 42
10.6.2.1 Alternative 1: Dispensing Solder . . . 42
10.6.2.2 Alternative 2: Printing Solder . . . 43
10.7 Inspection . . . 43
10.8 Component Salvage . . . 43
10.9 Voids in the Solder Joints . . . 44
10.9.1 Expected Void Content and Reliability . . . 44
10.9.2 Parameters with an Impact on Voiding . . . 44

11 Terminology . . . 46

12 References . . . 50

List of Figures

Figure 1 Simplified Block Diagram of PAN1322-SPP . . . 9
Figure 2 Pin Configuration for PAN1322-SPP in Top View (footprint) . . . 9
Figure 3 System Architecture Example of a Bluetooth System using eUniStone . . . 13
Figure 4 UART Interface . . . 16
Figure 5 UARTCTS Response Time . . . 17
Figure 6 Package Marking . . . 29
Figure 7 Production Package . . . 29
Figure 8 Top View and Bottom View . . . 30
Figure 9 Reference Design Schematics . . . 31
Figure 10 Cutout Drawing . . . 33
Figure 11 Equipment Label . . . 34
Figure 12 Declaration of Conformity . . . 35
Figure 13 Pad Layout on the Module (top view) . . . 37
Figure 14 Cutout Drawing . . . 38
Figure 15 Pin Marking . . . 39
Figure 16 Tape on Reel . . . 40
Figure 17 Eutectic Lead-Solder Profile . . . 41
Figure 18 Eutectic Leadfree-Solder Profile . . . 41
Figure 19 Solder Printing . . . 43
Figure 20 X-ray Picture Showing Voids Conforming to IPC-A-610D . . . 44

List of Tables

Table 1 Pin Description . . . 10
Table 2 UART Baud Rates . . . 16
Table 3 Default (non-inverted) behavior of UART signals . . . 17
Table 4 Order Code as of 2013-05-14 . . . 18
Table 5 Absolute Maximum Ratings . . . 21
Table 6 Operating Conditions . . . 21
Table 7 Internal1 (1.5 V) Supplied Pins . . . 22
Table 8 Internal2 (2.5 V) Supplied Pins . . . 22
Table 9 VDDUART Supplied Pins . . . 22
Table 10 VDD1 Supplied Pins . . . 23
Table 11 ONOFF PIN . . . 23
Table 12 Pull-up and Pull-down Currents . . . 24
Table 13 Max. Load at the Different Supply Voltages . . . 25
Table 14 BDR - Transmitter Part . . . 25
Table 15 BDR - Receiver Part . . . 26
Table 16 EDR - Transmitter Part . . . 27
Table 17 EDR -Receiver Part . . . 27

1 General Device Overview

1.1 Features

General

- Complete Bluetooth 2.1 + EDR solution
- Implements a single point-to-point data link to other SPP capable Bluetooth devices
- Ultra low power design in 0.13 µm CMOS
- Temperature range from -40°C to 85°C
- Integrates ARM7TDMI, RAM and patchable ROM
- On-module voltage regulators. External supply 2.9 - 4.1 V
- On-module EEPROM with configuration data
- On-module tuned reference clock
- Module can enter low power mode in idle state and during sniff intervals

Interfaces

- AT command interface over UART with HW flow control
- Default UART baudrate 115200 bit/s
- Module configuration reprogrammable for 9600 bit/s up to 3.25 Mbit/s UART baudrate
- JTAG for boundary scan in production test

RF

- Class 2 device up to +4 dBm
- Receiver sensitivity typ. -86 dBm
- Integrated antenna, balun and ISM band filter
- Integrated LNA with excellent blocking and intermodulation performance
- Digital demodulation for optimum sensitivity and co-/adjacent channel performance

Bluetooth

- Bluetooth V2.1 + EDR compliant
- Secure Simple Pairing
- Device A (initiating link) or Device B (accepting link) role supported
- Single point-to-point data link, role switch supported
- Packet data mode and stream data mode supported
- Sniff mode and Sniff Subrating is supported with above capabilities
- 5 trusted devices stored in EEPROM
- SW version available to configure specific RF certification tests

1.2 Block Diagram

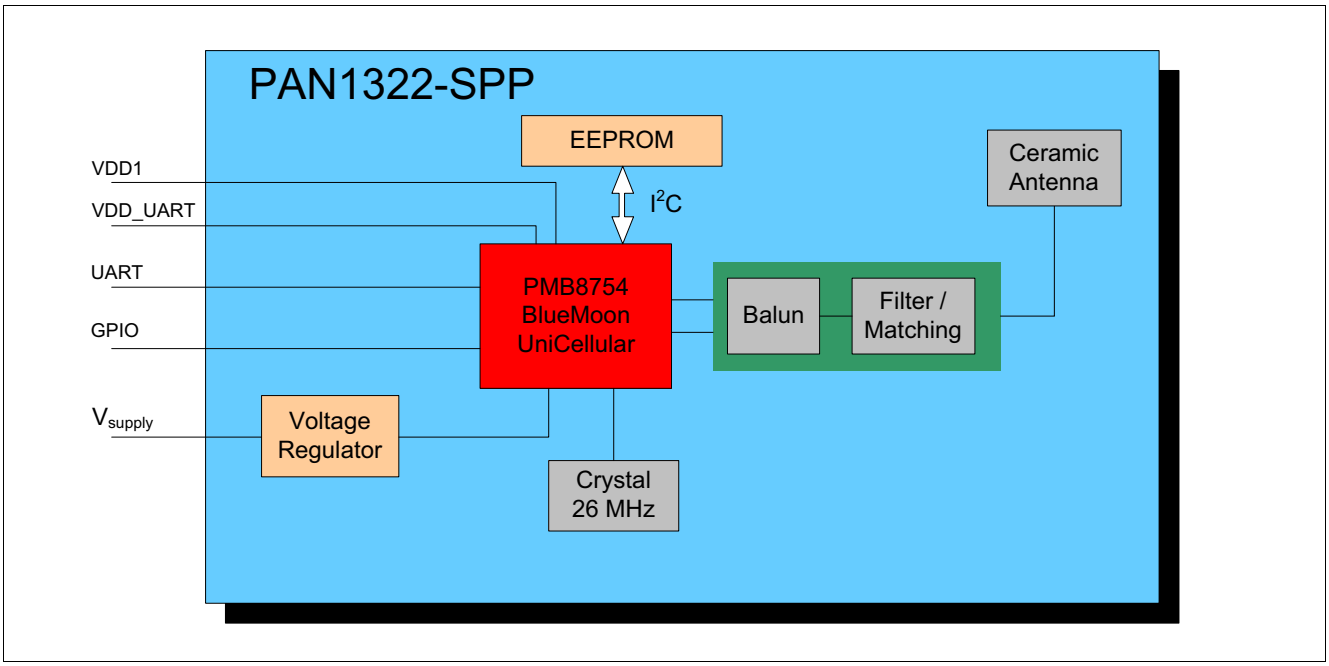

Figure 1 Simplified Block Diagram of PAN1322-SPP

1.3 Pin Configuration LGA

Figure 2 Pin Configuration for PAN1322-SPP in Top View (footprint)

1.4 Pin Description

The non-shaded cells indicate pins that will be fixed for the product lifetime. Shaded cells indicate that the pin might be removed/changed in future variants. Pins not listed below shall not be connected.

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
A2	P1.6	I/O/OD	Internal1	Z	Z	Port 1.6
A3	RESET#	AI	Internal1	Input	Input	Hardware Reset, active low
A8	P1.5	I/O/OD	Internal1	Input	Input	Port 1.5
B1	P1.7	I/O/OD	Internal1	PD/ Input	PD/ Input	Port 1.7
B2	P1.8	I/O/OD	Internal1	PD	PD	Port 1.8
B3	P1.0 / TMS	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.0 or JTAG interface
B4	P1.4 / RTCK	I/O/OD	Internal2	Z	Z	Port 1.4 or JTAG interface
B5	ONOFF	I		-	-	Connect to VDD1 and refer to chapter 12 item [3].
B9	SLEEPX	I/O	VDDUART	PD	H	Sleep indication signal
C2	P0.9	I/O/OD	Internal2	Z	Z	Port 0.9
C3	JTAG#	I	Internal2	PU	PU	Mode selection Port 1: 0: JTAG 1: Port
C4	TRST#	I	Internal2	PD	PD	JTAG interface
D1	P0.10	I/O/OD	Internal2	Z	Z	Port 0.10
D2	P0.8	I/O/OD	Internal2	PD	PD	Port 0.8
D3	P1.1 / TCK	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.1 or JTAG interface
D4	P0.3	I/O/OD	VDD1	Conf. PD def.	Conf. PD def.	Port 0.3
D5	P0.2	I/O/OD	VDD1	Z	Z	Port 0.2
E1	P0.12 / SDA0	I/O/OD	Internal2	PU	PU	I2C data signal
E2	P0.13 / SCL0	I/O/OD	Internal2	PU	PU	I2C clock signal
E3	P1.3 / TDO	I/O/OD	Internal2	Z	Z	Port 1.3 or JTAG interface
E4	P0.0	I/O/OD	VDD1	PD	PD	Port 0.0 LPM wakeup output
E5	P0.1	I/O/OD	VDD1	PD	PD	Port 0.1
E6	P0.5 / UARTRXD	I/O/OD	VDDUART	Z	Z	Port 0.5 or UART receive data
F2	P1.2 / TDI	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.2 or JTAG interface
F3	P0.11	I/O/OD	Internal2	Z	Z	Port 0.11

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
F4	P0.14 LPmin	I/O	VDDUART	Z	Z	Port 0.14 LPM wakup input
F5	P0.7 / UARTCTS	I/O/OD	VDDUART	Z	Z	Port 0.7 or UART CTS flow control
F7	P0.4 / UARTTXD	I/O/OD	VDDUART	PU	PU	Port 0.4 or UART transmit data
F8	P0.6 / UARTRTS	I/O/OD	VDDUART	PU	PU	Port 0.6 or UART RTS flow control
A4, A5, A6	VSUPPLY	SI		-	-	Power supply
C1	VREG	SO		-	-	Regulated Power supply
F6	VDDUART	SI		-	-	UART interface Power supply
C5	VDD1	SI		-	-	Power supply
A1, A7, A9, A11, A12, C8, C9, D7, D8, E8, E9, F1, F9 F11, F12	VSS			-	-	Ground
B6, B7, B8, C6, C7, D6, D9, E7	NC	-	-	-	-	No connection

1) Fixed pull-up/pull-down if JTAG interface is selected, not affected by any chip reset. If JTAG interface is not selected the port is tristate.

Descriptions of acronyms used in the pin list:

Acronym	Description
I	Input
O	Output
OD	Output with open drain capability
Z	Tristate
PU	Pull-up
PD	Pull-down
A	Analog (e.g. AI means analog input)
S	Supply (e.g. SO means supply output)

1.5 System Integration

PAN1322-SPP is optimized for a low bill of material (BOM) and a small PCB size. **Figure 3** shows a typical application example.

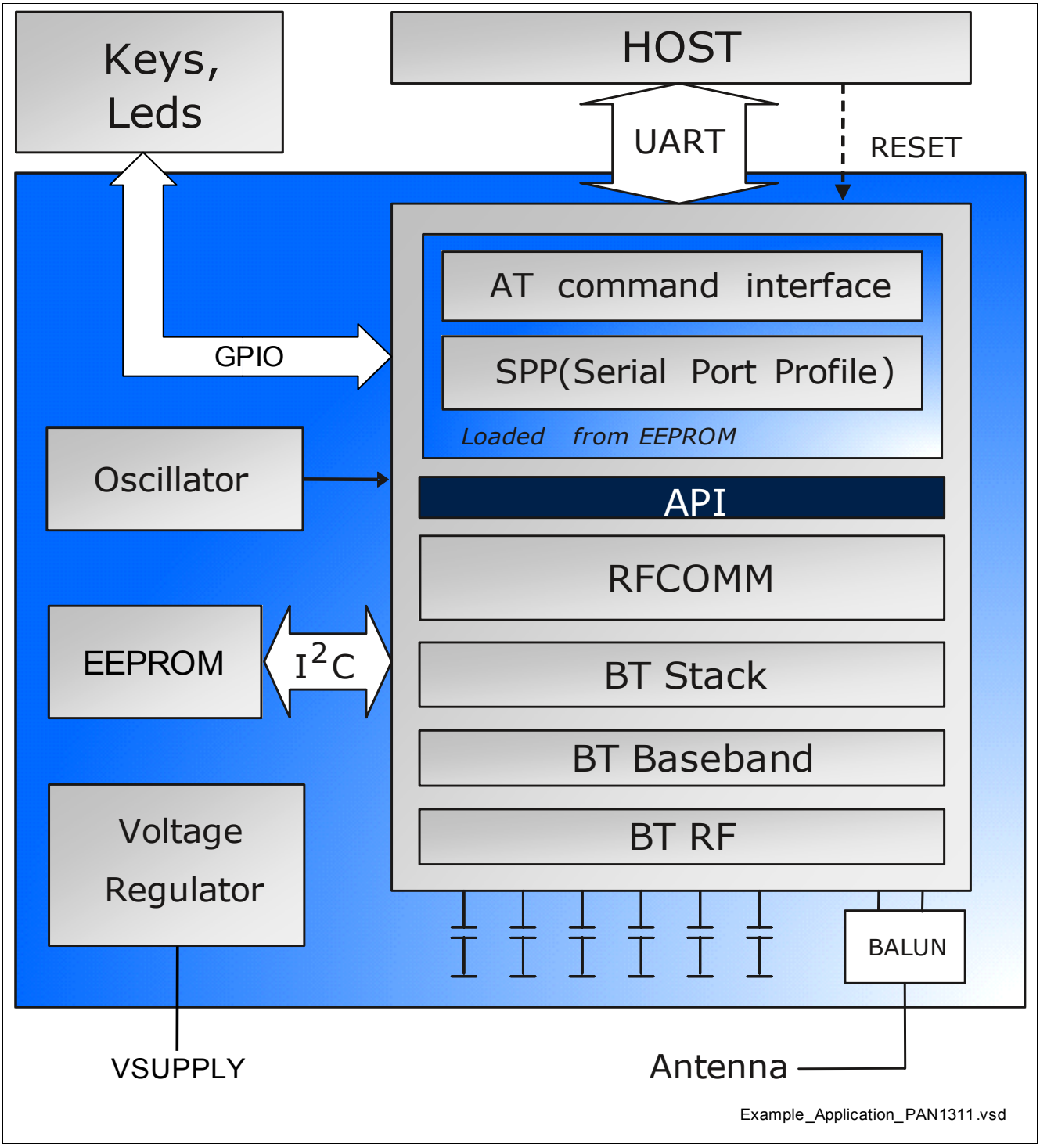

Figure 3 System Architecture Example of a Bluetooth System using eUniStone

The UART interface is used for communication between the host and PAN1322-SPP. The lines UARTTXD and UARTRXD are used for commands, events and data. The lines UARTRTS and UARTCTS are used for hardware flow control.

Low power mode control of PAN1322-SPP and the host can be implemented in by using the pins P0.14 and P0.0. P0.14 is used by the host to allow PAN1322-SPP to enter low power mode and P0.0 is used by PAN1322-SPP to wake-up the host when attention is required. Additionally, the host could hardware reset PAN1322-SPP using the RESET# pin.

Power is supplied to a single VSUPPLY input from which internal regulators can generate all required voltages. The UART and the GPIO's interfaces have separate supply voltages so that they can comply with host signaling.

1.6 SW Patch in EEPROM

Bug fixes for the SW in ROM are downloaded from the EEPROM. Panasonic may include new bug fixes in EEPROM during product lifetime.

1.7 FW Version

PAN1322-SPP is available in different firmware (FW) versions. Please check corresponding release documents for latest information in item **[2]**.

The identifier about the software version will be visible on the module, please refer to **Figure 6**, here it is the identifier SW (Software). For example SW01 match with FW3.1.

2 Basic Operating Information

2.1 Power Supply

PAN1322-SPP is supplied from a single supply voltage VSUPPLY. This supply voltage must always be present. The PAN1322-SPP chip is supplied from an internally generated 2.5 V supply voltage. This voltage can be accessed from the VREG pin. This voltage may not be used for supplying other components in the host system but can be used for referencing the host interfaces.

The GPIO's and the UART interface are supplied with dedicated, independent, reference levels via the VDD1 and VDDUART pins. All other digital I/O pins are supplied internally by either 2.5 V (Internal2) or 1.5 V (Internal1). **Section 1.4** provides a mapping between pins and supply voltages.

The I/O power domains (VDD1 and VDDUART) are completely separated from the other power domains and can stay present also in low power modes.

2.2 Clocking

PAN1322-SPP contains a crystal from which the internal 26 MHz system clock is generated. Also, the low power mode clock of 32,768 kHz is generated internally, which means that no external clock is needed.

2.3 Low Power Modes

To minimize current consumption, eUniStone automatically switches between different low power modes. The major modes are described below.

2.3.1 Low Power Mode

In Low Power Mode (LPM) most parts of eUniStone are powered down. This is done automatically in idle mode or if the link is in Sniff mode and the host allows LPM with the pin P0.14.

2.3.2 Complete Power Down

If Bluetooth functionality is not needed at all, VSUPPLY should be grounded to minimize power consumption. In this state there is no activity in eUniStone and the Bluetooth state (native clock, etc.) is not updated.

2.3.3 ON/OFF

PAN1322-SPP provides an alternative way to power down using the ONOFF logic input. When the ONOFF is low, the internal regulator on the module is turned OFF. The intention with the signal is to have the possibility to turn off the module without having to turn off the supply voltage. In the OFF state, the module will consume less than 1mA excluding the interface currents that is mainly set by the external load.
If this signal isn't used then it should be connected to VSUPPLY on the host PCB.

3 PAN1322-SPP Interfaces

3.1 UART Interface

The UART interface is the main communication interface between the host and PAN1322-SPP. AT commands are desribed in detail in the AT Commands specification [1].

The interface consists of four UART signals and two LPM control signals as shown in Figure 4.

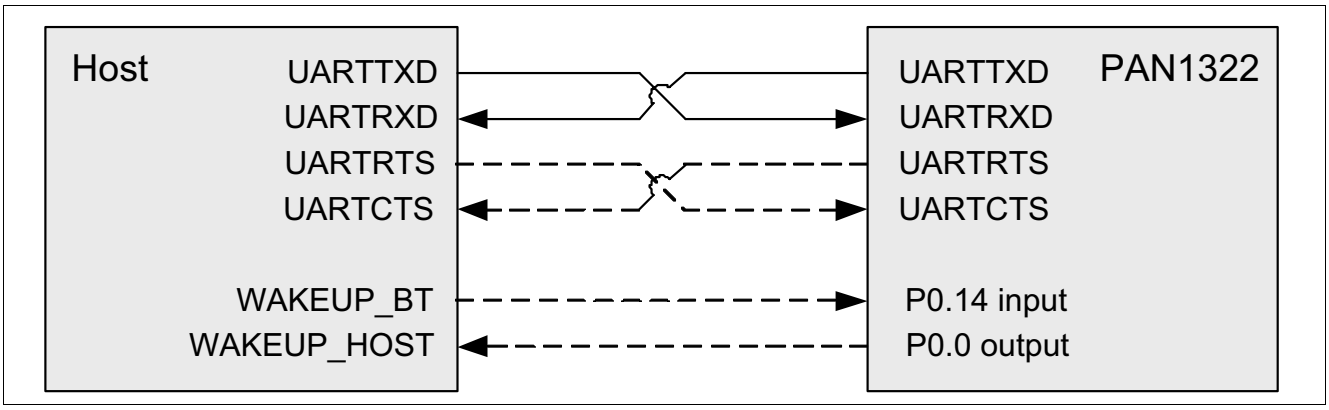

Figure 4 UART Interface

3.1.1 UART

The lines UARTTXD and UARTRXD are used for commands, responses and data. The lines UARTRTS and UARTCTS are used for hardware flow control. A separate supply voltage, VDDUART, defines the UART reference levels to fit any system requirements.

3.1.1.1 Baud Rates

The UART baud rate can be configured with the BD_DATA parameter *UART_Baudrate*. The module is programmed for a default baudrate of 115200 baud. Reprogramming of the EEPROM configuration is possible by AT commands at manufacturing time of the end product. The baudrate written to EEPROM will be used each time PAN1322-SPP starts or, HW or SW reset is done.

The host is also able to change the baudrate temporarily with an AT command. This baudrate is used by PAN1322-SPP until a HW or SW reset is done, when it will change back to the baudrate stored in the EEPROM.

The supported baud rates are listed in Table 3 together with the small deviation error that results from the internal clock generation.

Table 2 UART Baud Rates

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
9600	9615	0.16
19200	19230	0.16
38400	38461	0.16
57600	57522	-0.14
115200	115044	-0.14
230400	230088	-0.14
460800	464285	0.76
921600	928571	0.76

Table 2 UART Baud Rates (cont'd)

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
1843200	1857142	0.76
3250000	3250000	0

3.1.1.2 Detailed UART Behavior

After reset the UART interface is configured with one start bit, eight data bits, no parity bit and one stop bit. The least significant bit is transmitted first.

The polarity of the UART signals can be changed with the BD_DATA parameter UART_Invert. The default (non-nverted) behavior is shown in **Table 4**.

Table 3 Default (non-inverted) behavior of UART signals

Signal	Level	Meaning
UARTTXD / UARTRXD	0	Start bit, '0' bit in character.
	1	Idle level, stop bit
UARTRTS / UARTCTS	0	Flow on
	1	Flow stopped

3.1.1.3 UARTCTS Response Time

Figure 5 shows the UARTCTS response time. Assuming non-inverted UART signals, the data flow stops within the "flow off response time" after UARTCTS has been set to high. If UARTCTS goes high during the transmission of a byte (phase 1 in the figure) this byte will be completely transmitted. While UARTCTS is high, no data will be transmitted (phase 2). When UARTCTS goes low again, data transmission will continue (phase 3).

The maximum flow off response time is 10 UART bits (including start and stop bits). As an example, if the UART baud rate is 115200 Baud, the maximum flow off response time is 10 x 1/115200 s = 87 µs.

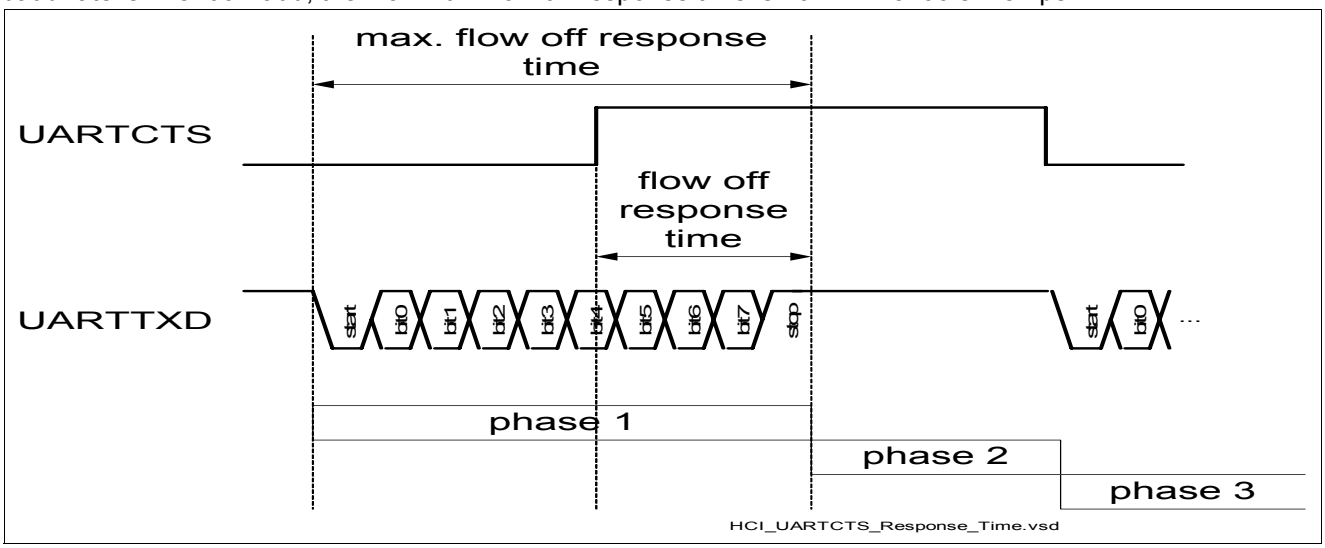

Figure 5 UARTCTS Response Time

3.2 Low Power Control

Pin P0.14 and P0.0 are optional, but strongly recommended to be used. P0.14 is used to allow PAN1322-SPP to enter Low Power Mode (LPM). P0.0 is used by PAN1322-SPP when in LPM to wake up the host.

4 General Device Capabilities

This chapter describes features available in the PAN1322 (ENW89841A3KF) core.

Actual feature set and how to access the features can be found in the AT Command document [1]. Release specific performance characteristics, like data speed, is related in the SW Release Notes [2].

4.1 RF Test Application

The PAN1322 module can be programmed over UART with a specific application for RF test purposes, e.g. TX continuous or TX burst mode. This test application is controlled over the UART through Intel specific HCI commands. The commands supported by this test application are described in the document “T8753-2-Infineon_Specific_HCI_Commands-7600.pdf”.

4.2 Firmware ROM Patching

In any chip with complex firmware in ROM it is wise to support patching. The risk of project delay is significantly reduced when problems can be solved without hardware changes. Enhancements, adaptations and bug fixes can be handled very late during design-in, even after the PAN1322 has been soldered in the final product.

The well-proven patch concept used in PAN1322 is described below.

4.2.1 Patch Support

PAN1322-SPP contains dedicated hardware that makes it possible to apply patches to the code and data in the firmware ROM. The hardware is capable of replacing up to 32 blocks of 16 bytes each with new content. This area can be filled with any combination of code and data. The firmware patch is stored in EEPROM and automatically loaded after startup. This provides a flexible bugfix solution for the ROM part of the firmware.

5 Ordering Information

This chapter shows the different order codes for the PAN1322-SPP. In case, there is no specific software version mentioned in the order, we will always deliver the latest official software release, which is downwards compatible. Please refer also to Table 2 “Firmware Releases as of 2013-05-14” on Page 14.

Table 4 Order Code as of 2013-07-03

Order Code	Description	MOQ [1)]
ENW89841A3KF	PAN1322-SPP Bluetoth 2.1 Module with integrated Antenna and a standard SPP software.	1500

1) Abbreviation for Minimum Order Quantity (MOQ). The standard MOQ for mass production are 1500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity.

6 Bluetooth Capabilities

6.1 Supported Features

- Bluetooth V2.1 + EDR compliant
- Enhanced Data Rate 2 and 3 Mbit/s symbol rate on the air
- Secure Simple Pairing
- Device A (initiating link) or Device B (accepting link) role supported
- Single point-to-point data link, role switch supported
- Packet data mode and stream data mode supported
- Link in sniff mode supported. Device enters Low Power Mode in sniff intervals if permitted by the host.
- Sniff Subrating
- 5 trusted devices stored in EEPROM
- Connection to a Bluetooth Tester

6.2 PAN1322-SPP Bluetooth Features

6.2.1 Secure Simple Pairing

The device implements Secure Simple Pairing with the following association models according to BT2.1 core specification:

- Numeric Comparisoon
- Just Works
- Passkey Entry

Also pairing with legacy (BT2.0 and older) devices is supported.

6.2.2 Role Switch

The initiating device (devA) starts as Bluetooth master of the link, the accepting device starts as Bluetooth slave of the link. The remote device can request a role change to accomodate with other Bluetooth links. If that happens, the module will send an event to the host. Also if the PAN1322-SPP start as slave, (Device B), the other device can change it's own role making PAN1322-SPP master. The host controlling PAN1322-SPP will be notified with the same event.

6.2.3 Sniff Mode

The local host or the remote device can request sniff mode for the link. During sniff mode, the devices synchronize on sniff instants only. The module will enter low power mode in the sniff intervals, if allowed by the host LPM control signals. Data packets can be exchanged at the sniff instants only, so the data rate is reduced in sniff mode. The module will wake up the host when data is received or other responses need to be transmitted.

6.2.4 Sniff Subrating

The local host or the remote device can request Sniff Subrating for the link. When in sniff mode, the device will automatically switch between Sniff Mode and Sniff Subrating Mode making it possible to stay longer in Low Power Mode when there is no data transmitted or received.

6.2.5 Enhanced Power Control

PAN1322-SPP support Enhanced Power Control according to Bluetooth specification 3.0. The Enhanced Power Control is handled automatically to make different modulations modes transmit on optimal levels.

6.2.6 Encryption Pause and Resume

Encryption Pause Resume is supported making it possible to change connection link key on an encrypted link, pause the encryption and resume it with the new link key. This is handled automatically by PAN1322-SPP to make the link more secure.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature		-40	–	125	°C	–
VSUPPLY supply voltage		-0.3	–	6.0	V	–
VDDUART supply voltage		-0.9	–	4.0	V	–
VDD1 supply voltage		-0.9	–	4.0	V	–
VREG		-0.3	–	4.0	V	VSUPPLY > 4 V
VREG		-0.3	–	VSUPPLY	V	VSUPPLY < 4 V
ONOFF		-0.3	–	VSUPPLY+0.3	V	
Input voltage range		-0.9	–	4.0	V	–
Output voltage range		-0.9	–	4.0	V	-9
ESD		–	–	1.0	kV	According to MIL-STD883D method 3015.7

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

7.2 Operating Conditions

Table 6 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operating temperature		-40	–	85	°C	–
Main supply voltage (Vsupply)		2.9	–	4.1[1)]	V	–
VDDUART		1.35	–	3.6	V	–
VDD1		1.35	–	3.6	V	–

1) At ambient temperatures above 65°C the maximum allowed power dissipation in the module is limited to 200 mW

7.3 DC Characteristics

7.3.1 Pad Driver and Input Stages

For more information, see **Chapter 1.4**.

Table 7 Internal1 (1.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.27	V	–
Input high voltage		1.15	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 1 mA
Output high voltage		1.1	–	–	V	IOH = -1 mA
Continuous Load[1)]		–	–	1	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal1 supplied pins shall not exceed 2mA at the same time

Table 8 Internal2 (2.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.45	V	–
Input high voltage		1.93	–	2.8	V	P0.10
Input high voltage		1.93	–	3.6	V	Other pins
Output low voltage		–	–	0.25	V	IOL = 5 mA
Output low voltage		–	–	0.15	V	IOL = 2 mA
Output high voltage		2.0	–	–	V	IOH = -5 mA
Output high voltage		2.1	–	–	V	IOH = -2 mA
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal2 supplied pins shall not exceed 35 mA at the same time

Table 9 VDDUART Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDDUART	V	–
Input high voltage		0.7*VDDUART	–	VDDUART+0.3	V	P0.5/UARTRXD
Input high voltage		0.7*VDDUART	–	3.6	V	Other pins

Table 9 VDDUART Supplied Pins (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output low voltage		–	–	0.25	V	IOL = 5 mA VDDUART = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.25	–	–	V	IOH = -5 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.15	–	–	V	IOH = -2 mA VDDUART = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDDUART supplied pins shall not exceed 35 mA at the same time

Table 10 VDD1 Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDD1	V	–
Input high voltage		0.7*VDD1	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 5 mA VDD1 = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.25	–	–	V	IOH = -5 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.15	–	–	V	IOH = -2 mA VDD1 = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDD1 supplied pins shall not exceed 35 mA at the same time

Table 11 ONOFF PIN

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		–	–	0.7	V	–
Input high voltage		1.7	–	VSUPPLY	V	–
Input current		-1	0.01	1	µA	ONOFF = 0 V

7.3.2 Pull-ups and Pull-downs

Table 12 Pull-up and Pull-down Currents

Pin	Pull Up Current			Pull Down Current			Unit	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
P0.12 P0.13	260	740	1300	N/A	N/A	N/A	µA	Pull-up current measured with pin voltage = 0 V Pull-down current measured with pin voltage = supply voltage Min measured at 125°C with supply = 1.35 V Typ. measured at 27°C with supply = 2.5V Max measured at -40°C with supply = 3.63 V
P0.0 P0.1 P0.2 P0.3	22	130	350	23	150	380	µA	
P0.4 P0.5 P0.6 P0.7 P0.10 P0.8 P0.9 P0.11 P0.14 P0.15	4.2	24	68	3.0	20	55	µA	
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7 P1.8	1.1	6.0	17	0.75	5.0	14	µA	

7.3.3 Protection Circuits

All pins have an inverse protection diode against VSS.
P0.10 has an inverse diode against Internal2.
P0.5/UARTRXD has an inverse diode against VDDUART.
All other pins have no diode against their supply.

7.3.4 System Power Consumption

Table 13 Max. Load at the Different Supply Voltages

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Vsupply		–	–	100	mA	Peak current

Note: I/O currents are not included since they depend mainly on external loads. For more details see ***[2]***.

7.4 RF Part

7.4.1 Characteristics RF Part

The characteristics involve the spread of values to be within the specific temperature range. Typical characteristics are the median of the production.

All values refers to Panasonic reference design.

7.4.1.1 Bluetooth Related Specifications

Table 14 BDR - Transmitter Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output power (high gain)		0.5	2.5	4.5	dBm	Default settings
Output power (highest gain)		–	4.5	–	dBm	Maximum settings
Power control step size		4	6	8	dB	–
Frequency range fL		2400	2401.3	–	MHz	–
Frequency range fH		–	2480.7	2483.5	MHz	–
20 dB bandwidth		–	0.930	1	MHz	–
2nd adjacent channel power		–	-40	-20	dBm	–
3rd adjacent channel power		–	-60	-40	dBm	–
>3rd adjacent channel power		–	-64	-40	dBm	Max. 2 of 3 exceptions @ 52 MHz offset might be used
Average modulation deviation for 00001111 sequence		140	156	175	kHz	–
Minimum modulation deviation for 01010101 sequence		115	145	–	kHz	–
Ratio Deviation 01010101 / Deviation 00001111		0.8	1	–		–
Initial carrier frequency tolerance |foffset|		–	–	75	kHz	–
Carrier frequency drift (one slot) |fdrift|		–	10	25	kHz	–
Carrier frequency drift (three slots) |fdrift|		–	10	40	kHz	–

Table 14 BDR - Transmitter Part (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Carrier frequency drift (five slots) |fdrift|		–	10	40	kHz	–
Carrier frequency driftrate (one slot) |fdriftrate|		–	5	20	kHz/50 ms	–
Carrier frequency driftrate (three slots) |fdriftrate|		–	5	20	kHz/50 ms	–
Carrier frequency driftrate (five slots) |fdriftrate|		–	5	20	kHz/50 ms	–

Table 15 BDR - Receiver Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sensitivity		–	-86	-81	dBm	Ideal wanted signal
C/I-performance: -4th adjacent channel		–	-51	-40	dB	–
C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-46	-20	dB	–
C/I-performance: -2nd adjacent channel (image)		–	-35	-9	dB	–
C/I-performance: -1st adjacent channel		–	-4	0	dB	–
C/I-performance: co. channel		–	9	11	dB	–
C/I-performance: +1st adjacent channel		–	-4	0	dB	–
C/I-performance: +2nd adjacent channel		–	-40	-30	dB	–
C/I-performance: +3rd adjacent channel		–	-50	-40	dB	–
Blocking performance 30 MHz - 2 GHz		10	–	–	dBm	Some spurious responses, but according to BT-specification
Blocking performance 2 GHz - 2.4 GHz		-27	–	–	dBm	–
Blocking performance 2.5 GHz - 3 GHz		-27	–	–	dBm	–
Blocking performance 3 GHz - 12.75 GHz		10	–	–	dBm	Some spurious responses, but according to BT-specification
Intermodulation performance		-39	-34	–	dBm	Valid for all intermodulation tests
Maximum input level		-20	–	–	dBm	–

Table 16 EDR - Transmitter Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output power (high gain)		-2.5	–	2	dBm	
Relative transmit power: PxPSK - PGFSK		-4	-0.6	1	dB	
Carrier frequency stability |ωi|		–	–	75	kHz	–
Carrier frequency stability |ωi+ω0|		–	–	75	kHz	–
Carrier frequency stability |ω0|		–	2	10	kHz	–
DPSK - RMS DEVM		–	10	20	%	–
8DPSK - RMS DEVM		–	10	13	%	–
DPSK - Peak DEVM		–	20	35	%	–
8DPSK - Peak DEVM		–	20	25	%	–
DPSK - 99% DEVM		–	–	30	%	–
8DPSK - 99% DEVM		–	–	20	%	–
Differential phase encoding		99	100	–	%	–
1st adjacent channel power		–	-40	-26	dBc	–
2nd adjacent channel power		–	–	-20	dBm	Carrier power measured at basic rate
3rd adjacent channel power		–	–	-40	dBm	Carrier power measured at basic rate

Table 17 EDR -Receiver Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DQPSK-Sensitivity		–	-88	-83	dBm	Ideal wanted signal
8DPSK-Sensitivityl		–	-83	-77	dBm	Ideal wanted signal
DQPSK - BER Floor Sensitivity		–	-84	-60	dBm	–
8DPSK - BER Floor Sensitivity		–	-79	-60	dBm	–
DQPSK - C/I-performance: -4th adjacent channel		–	-53	-40	dB	–
DQPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-47	-20	dB	–
DQPSK - C/I-performance: -2nd adjacent channel (image)		–	-31	-7	dB	–
DQPSK - C/I-performance: -1st adjacent channel		–	-7	0	dB	–
DQPSK - C/I-performance: co. channel		–	11	13	dB	–
DQPSK - C/I-performance: +1st adjacent channel		–	-9	0	dB	–

Table 17 EDR -Receiver Part (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DQPSK - C/I-performance: +2nd adjacent channel		–	-44	-30	dB	–
DQPSK - C/I-performance: +3rd adjacent channel		–	-50	-40	dB	–
8DPSK - C/I-performance: -4th adjacent channel		–	-48	-33	dB	–
8DPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-44	-13	dB	–
8DPSK - C/I-performance: -2nd adjacent channel (image)		–	-25	0	dB	–
8DPSK - C/I-performance: -1st adjacent channel		–	-5	5	dB	–
8DPSK - C/I-performance: co. channel		–	17	21	dB	–
8DPSK - C/I-performance: +1st adjacent channel		–	-5	5	dB	–
8DPSK - C/I-performance: +2nd adjacent channel		–	-36	-25	dB	–
8DPSK - C/I-performance: +3rd adjacent channel		–	-46	-33	dB	–
Maximum input level		-20	–	–	dBm	–

8 Package Information

8.1 Package Marking

Please refer to **"Ordering Information" on Page 18**

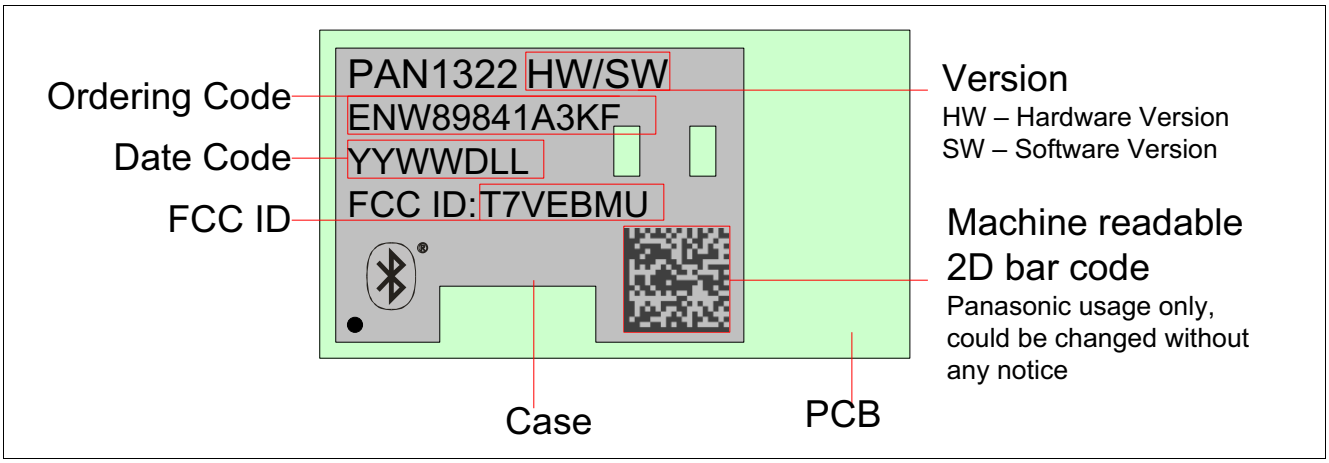

Figure 6 Package Marking

8.2 Production Package

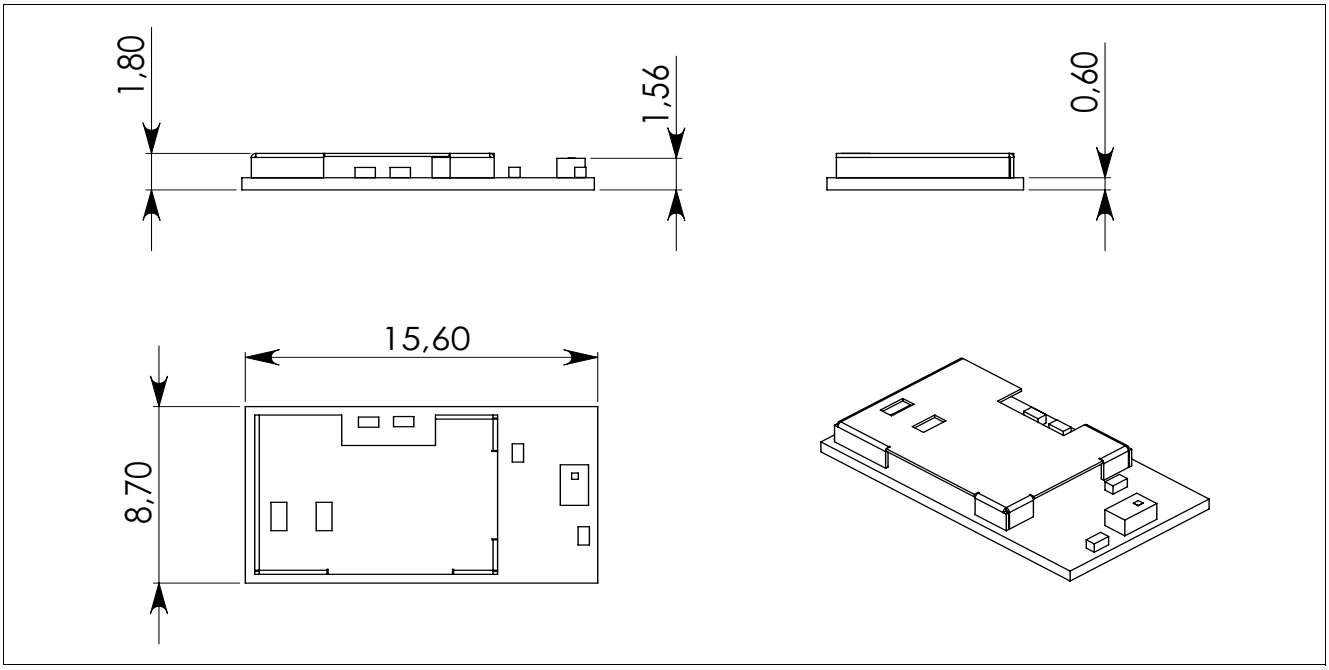

Figure 7 Production Package

All dimensions are in mm.

Tolerances on all outer dimensions, height, width and length, are +/- 0.2 mm.

8.2.1 Pin Mark

Pin 1 (A1) is marked on bottom footprint and on the top of the shield on the module according to **Figure 8**. Diameter of pin 1 mark on the shield is 0.40mm.

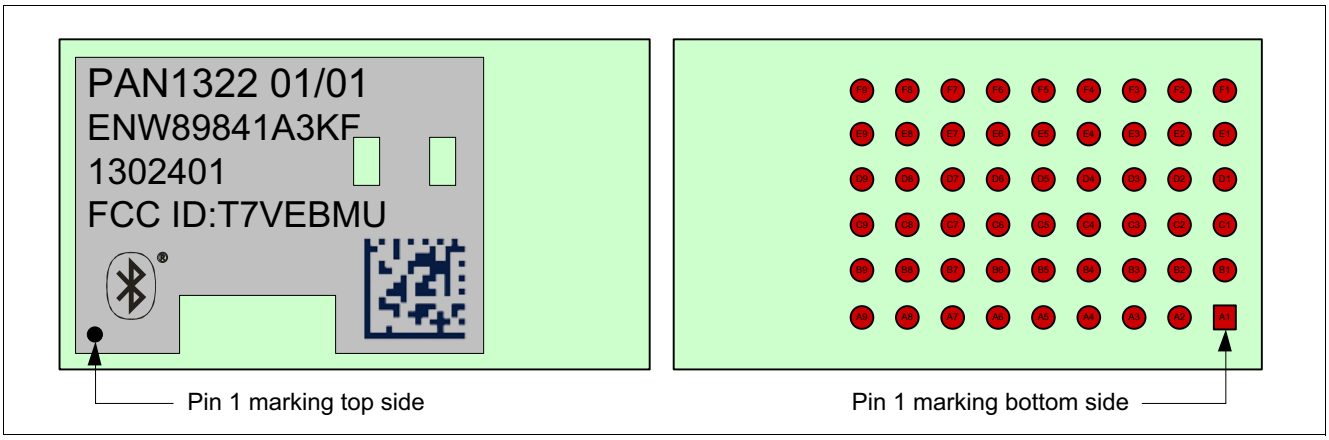

Figure 8 Top View and Bottom View

9 Bluetooth Qualification and Regulatory Certification

9.1 Reference Design

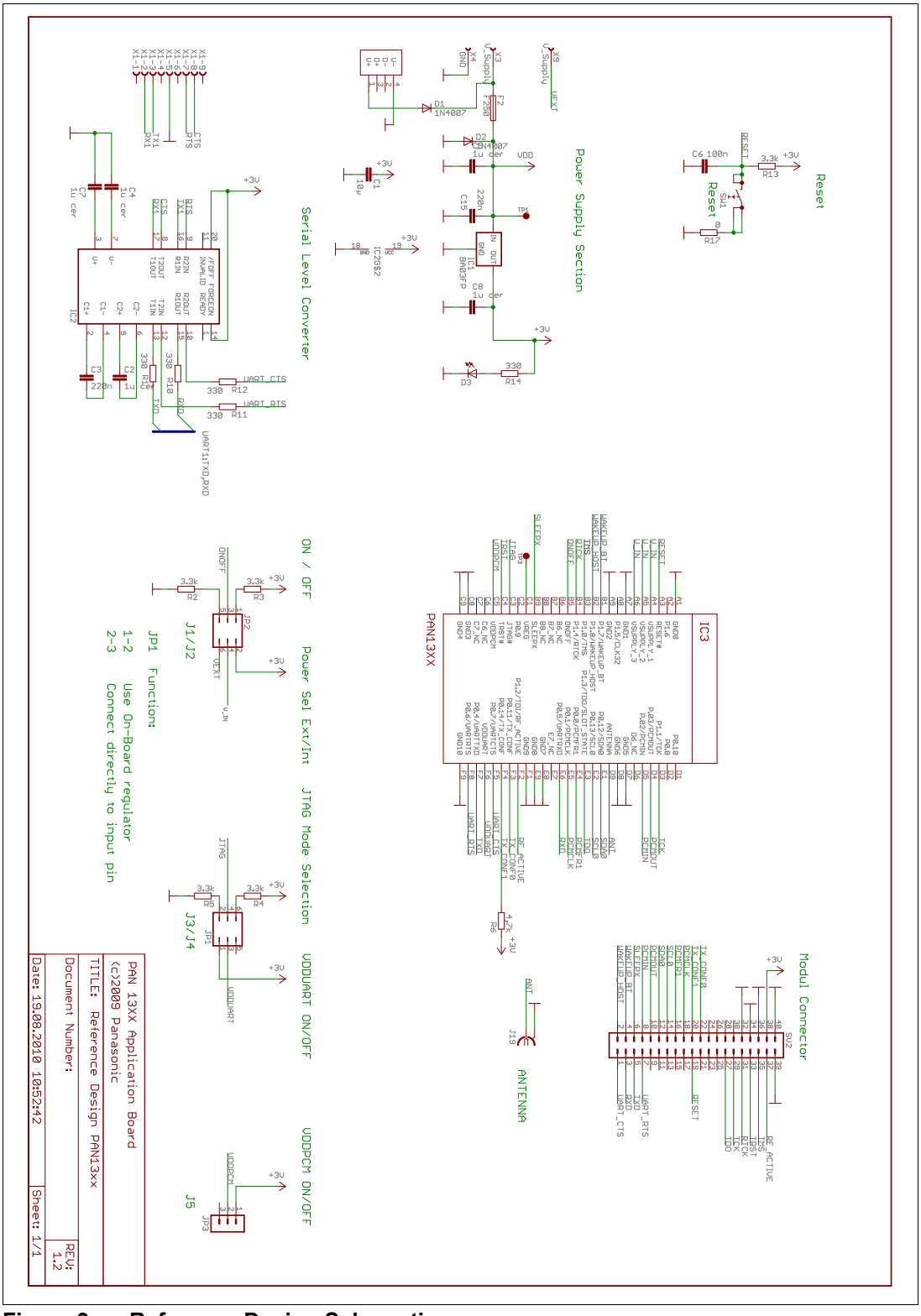

Figure 9 Reference Design Schematics

ENW89841A3KF is intended to be installed inside end user equipment. ENW89841A3KF is Bluetoooth-qualified and also FCC-certified and Industry Canada approved, and conforms to R&TTE (European) requirements and directives with the reference design described in **Figure 9**.

Manufacturers of mobile, fixed or portable devices incorporating this device are advised to clarify any regulatory questions and to have their complete product tested and approved for compliance (FCC or other when applicable). When using other antennas, a “class II permissive change” is required for FCC approval. The normal procedure is to first provide a technical test report showing that 4 dBi is not exceeded and to continue working with a regulatory test house to finalize the approval for a new antenna implementation.

There are no parts in ENW89841A3KF that can be modified by the user except modifications of the device BD data and loading of SW patches. Any changes or modifications made to this device that are not expressly approved by Panasonic, may void the user’s authority to operate the equipment.

9.2 FCC Class B Digital Devices Regulatory Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by 1 or more of the following measures:

- Reorient or relocate the antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio or television technician for help

9.3 FCC Wireless Notice

This product emits radio frequency energy, but the radiated output power of this device is far below the FCC radio frequency exposure limits. Nevertheless, the device should be used in such a manner that the potential for human contact with the antenna during normal operation is minimized.

To meet the FCC's RF exposure rules and regulations:

- The system antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
- The system antenna used for this module must not exceed 4 dBi.
- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance, please refer to **Figure 10**.

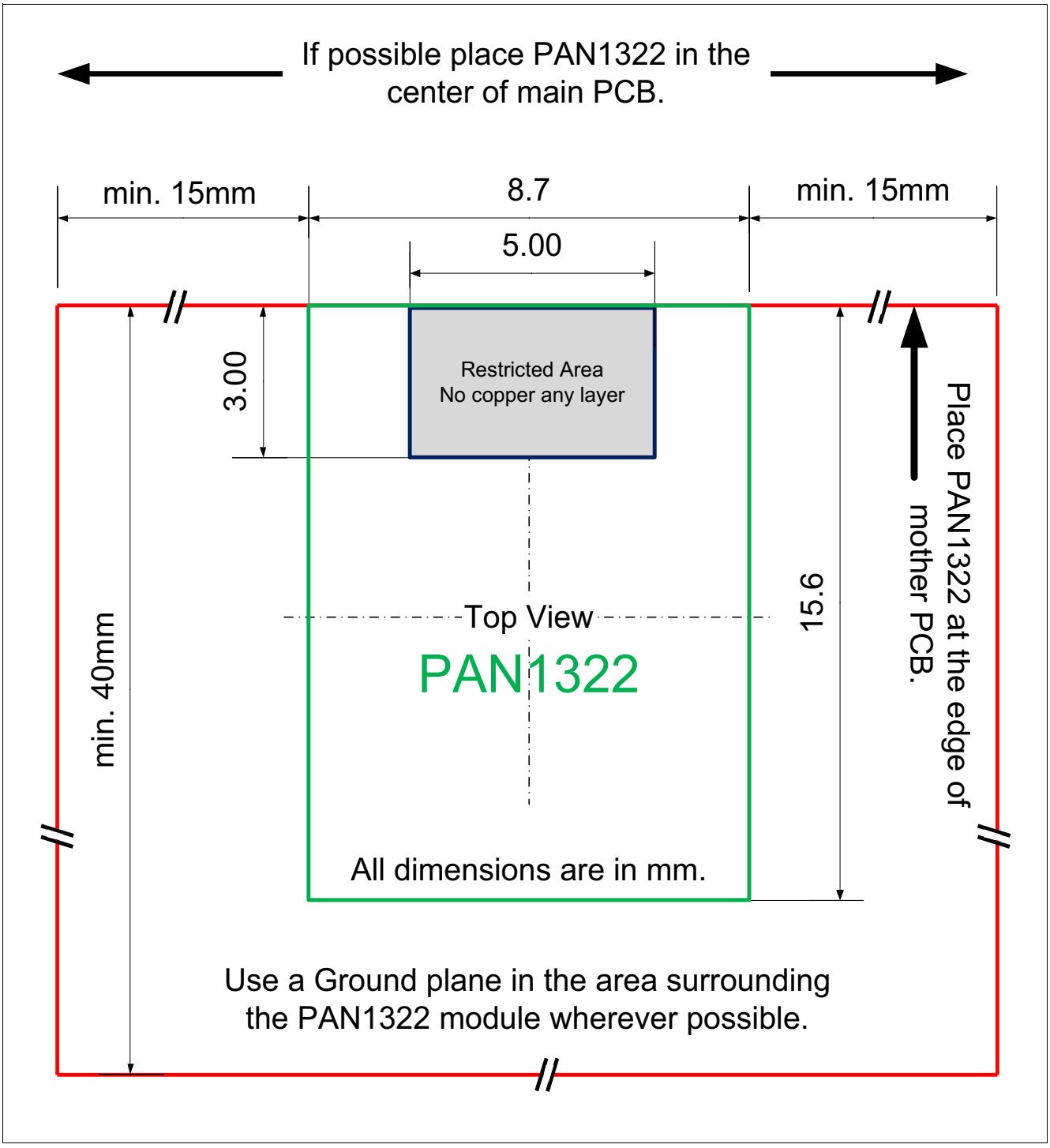

Figure 10 Cutout Drawing

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.

9.4 FCC Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference

2. This device must accept any interference received, including interference that may cause undesired operation.

9.5 FCC Identifier

FCC ID: T7VEBMU

9.6 European R&TTE Declaration of Conformity

Hereby, Panasonic Industrial Devices Europe GmbH, declares that the Bluetooth module ENW89841A3KF is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.

As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labelled as follows:

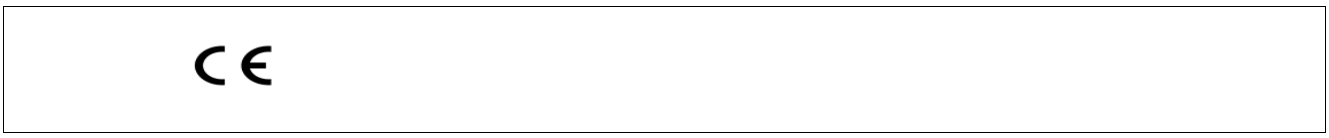

Figure 11 Equipment Label

PAN1322 in the specified reference design can be used in the following countries:

Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

Declaration of Conformity (DoC) 1999/5/EC

We, Panasonic Industrial Devices Europe GmbH
Wireless Connectivity, Power Electronics R&D Center
Zeppelinstrasse 19, 21337 Lueneburg, Germany

declare under our sole responsibility that the product:

Type of equipment: Bluetooth Module

Brand name: PAN1321 / PAN1311
PAN1322 / PAN1312

Model name: ENW89811K4CF / ENW89810K5CF
ENW89841A3KF / ENW89841C3KF

to which this declaration relates, is in compliance with all the applicable essential requirements, and other provisions of the European Council Directive:

1999/5/EC	Radio and Telecommunications Terminal Equipment Directive (R&TTE)

The conformity assessment procedure used for this declaration is Annex IV of this Directive.

Product compliance has been demonstrated on the basis of:

- EN 50371: 2002-11 - EN 60950-1: 2011-01	For article 3.1 (a) : Health and Safety of the User
- EN 301 489-1 V1.9.1 (2011-04) - EN 301 489-17 V2.1.1 (2009-05)	For article 3.1 (b) : Electromagnetic Compatibility
- EN 300 328 V1.7.1 (2006-10)	For article 3.2 : Effective use of spectrum allocated

The technical contruction file is kept available at:

Panasonic Industrial Devices Europe GmbH, Zeppelinstrasse 19, 21337 Lueneburg, Germany

Issued on: 31st of October 2012

Signed by the manufacturer:

(Company name) Panasonic Industrial Devices Europe GmbH

(Signature) Panasonic Industrial Devices Europe GmbH Zeppelinstraße 19 D - 21337 Lüneburg Tel.: +49 (0) 4131 / 899-0

(Printed name) Heino Kaehler

(Title) Manager Wireless Connectivity

Figure 12 Declaration of Conformity

9.7 Bluetooth Qualified Design ID

Panasonic has submitted End Product Listing (EPL) for PAN1322, based on Intel eBMU plattform, in the Qualified Product List of the Bluetooth SIG. These EPL are referring the Bluetooth qualfication of the SPP-AT application running on the eBMU chip under QD ID t.b.d.

Manufacturers of Bluetooth devices incorporating PAN1322 can reference the same QD ID number.

Bluetooth QD ID: t.b.d. (PAN1322 SPP BT2.0).

9.8 Industry Canada Certification

PAN1322 complies with the regulatory requirements of Industry Canada (IC), license: IC: 216Q-EBMU

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from **www.ic.gc.ca.**

This device has been designed to operate with the built in antenna. It is not allowed to alter the antenna or connecting an external antenna to the module. The built in antenna used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

9.9 Label Design of the Host Product

It is recommended to include the following information on the host product label:

Contains transmitter Module FCC ID: T7VEBMU / IC: 216QEBMU

9.10 Regulatory Test House

The test house used by Panasonic in the Bluetooth and Regulatory approvals for the module PAN1322:

Eurofins Product Service GmbH
Storkower Str. 38c
D-15526 Reichenwalde b. Berlin
GERMANY
Tel.: +49 33631 888 0
Fax: +49 33631 888 650
www.eurofins.com

10 Assembly Guidelines

The target of this chapter is to provide guidelines for customers to successfully introduce the PAN1322-SPP module in production. This includes general description, PCB-design, solder printing process, assembly, soldering process, rework and inspection.

10.1 General Description of the Module

PAN1322-SPP is a Land Grid Array (LGA 8.7mm x 15.6mm) module made for surface mounting. The pad diameter is 0.6 mm and the pitch 1.2 mm.

All solder joints on the module will reflow during soldering on the mother board. All components and shield will stay in place due to wetting force. Wave soldering is not possible.

Surface treatment on the module pads is Nickel (5 - 8 µm)/Gold (0.04 - 0.10 µm).

Figure 13 shows the pad layout on the module, seen from the component side.

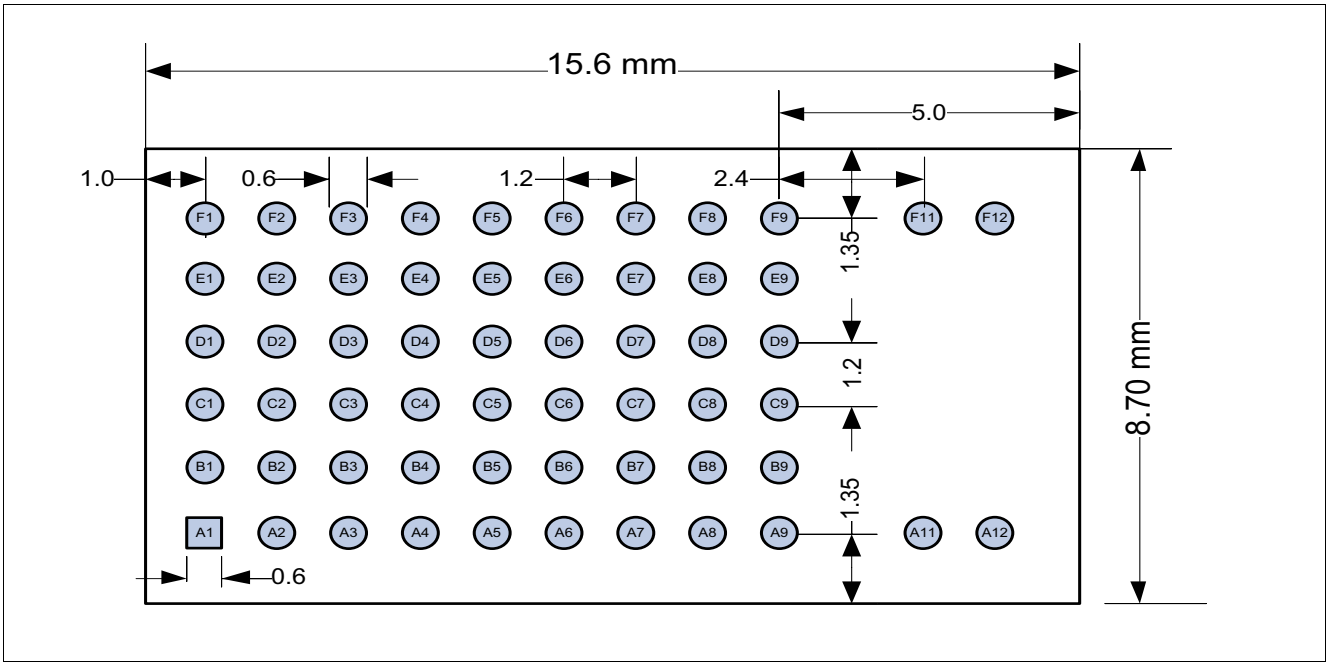

Figure 13 Pad Layout on the Module (top view)

10.2 Printed Circuit Board Design

The land pattern on the PCB shall be according to the land pattern on the module, which means that the diameter of the LGA pads on the PCB shall be 0.6 mm. It is recommended that each pad on the PCB shall be surrounded by a solder mask clearance of about 75 µm to avoid overlapping solder mask and pad.

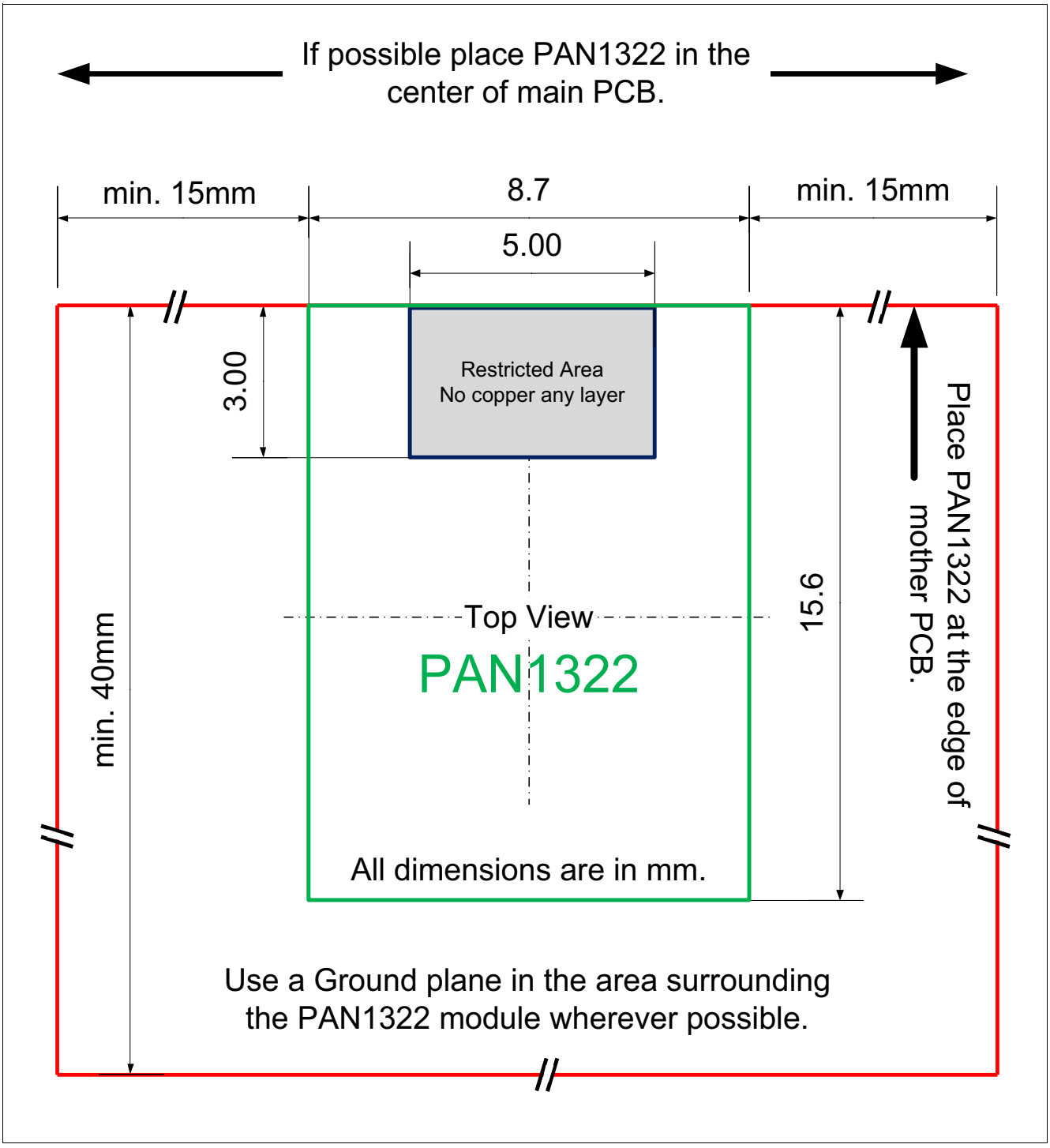

Figure 14 Cutout Drawing

In order to preserve the characteristics of the embedded antenna, a cutout must be respected under the antenna through all metal layers of the PCB, as shown in drawing **Figure 14**.

Placing the module inside a metal housing or close to metal parts like fasteners, shielding cages, washers, etc. can significantly affect the antenna characteristics.

10.3 Solder Paste Printing

The solder paste deposited on the PCB by stencil printing has to be of eutectic or near eutectic tin leadfree / lead composition. A no-clean solder paste is preferred, since cleaning of the solder joints is difficult because of the small gap between the module and the PCB.

Preferred thickness of the solder paste stencil is 100 - 127 µm (4 - 5 mils). The apertures on the solder paste stencil shall be of the same size as the pads, 0.6 mm.

10.4 Assembly

10.4.1 Component Placement

In order to assure a high yield, good placement on the PCB is necessary. As a rule of thumb the tolerable misplacement is 150 µm. This means that the PAN1322 module can be assembled with a variety of placement systems.

It is recommended to use a vision system capable of package pad recognition and alignment that evaluates the pad locations on the package (in contrast to outline centring). This eliminates the pad to package edge tolerance.

The recommendation is to pick and place the module with a nozzle in the centre of the shield. The nozzle diameter shall not be bigger than 4 mm.

10.4.2 Pin Mark

Pin 1 (A1) is marked on bottom footprint and on the top of the shield on the module according to **Figure 15**. Diameter of pin 1 mark on the shield is 0.40 mm.

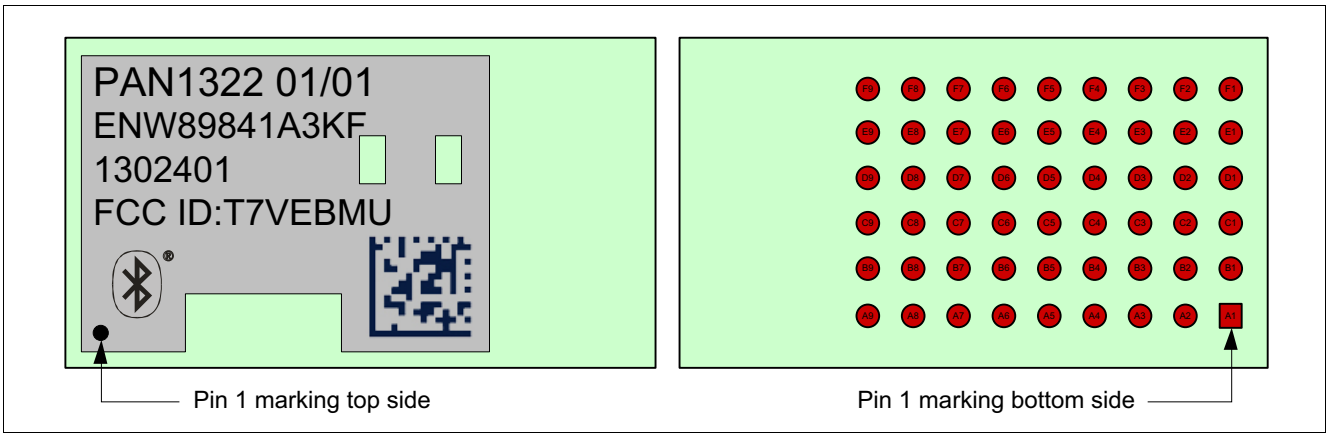

Figure 15 Pin Marking

10.4.3 Package

PAN1322 is packed in tape on reel according to **Figure 16**.

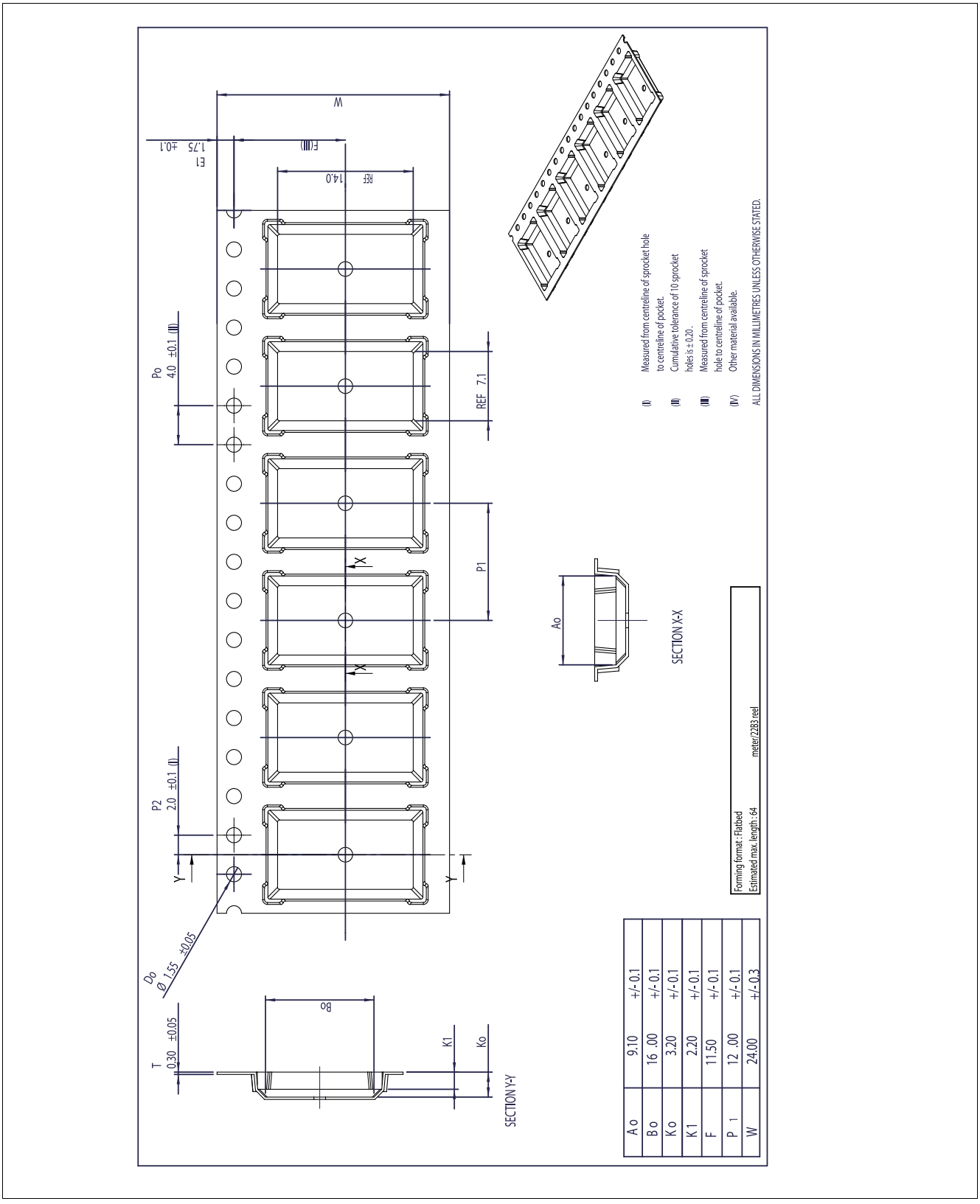

Figure 16 Tape on Reel

10.5 Soldering Profile

Generally all standard reflow soldering processes (vapour phase, convection, infrared) and typical temperature profiles used for surface mount devices are suitable for the PAN1322 module. **Wave soldering is not possible.**

Figure 17 and **Figure 18** shows example of a suitable solder reflow profile. One for leaded and one for leadfree solder.

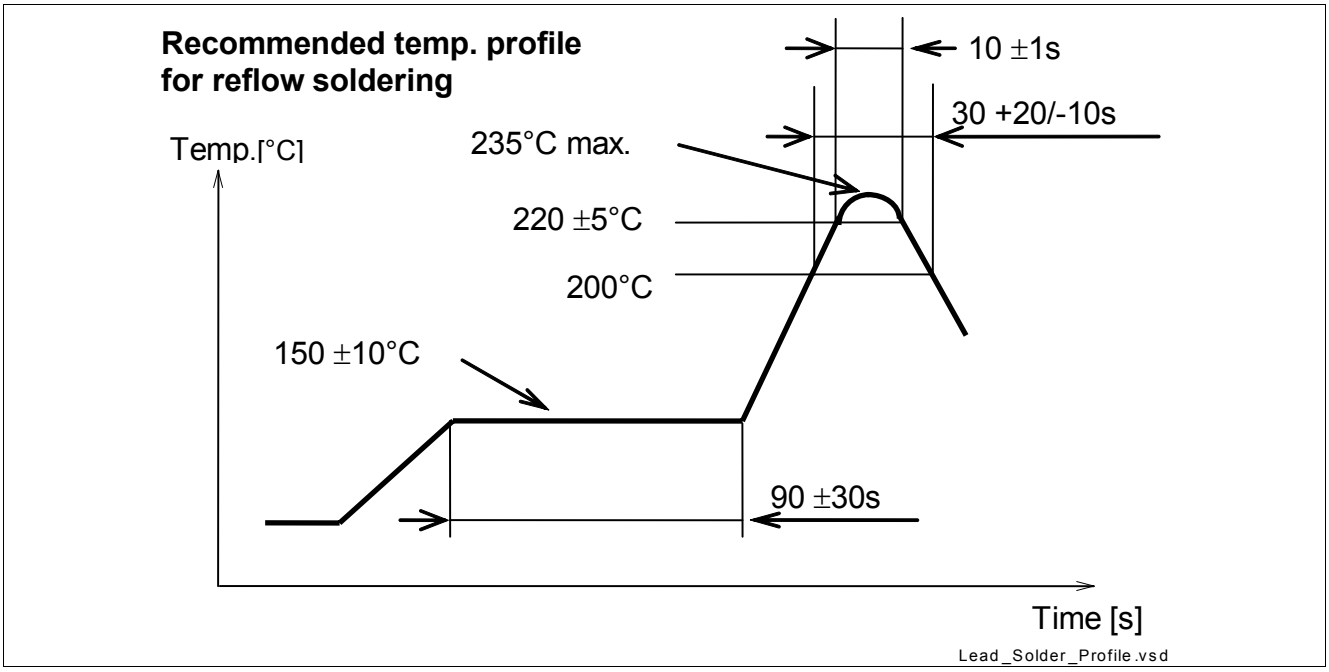

Figure 17 Eutectic Lead-Solder Profile

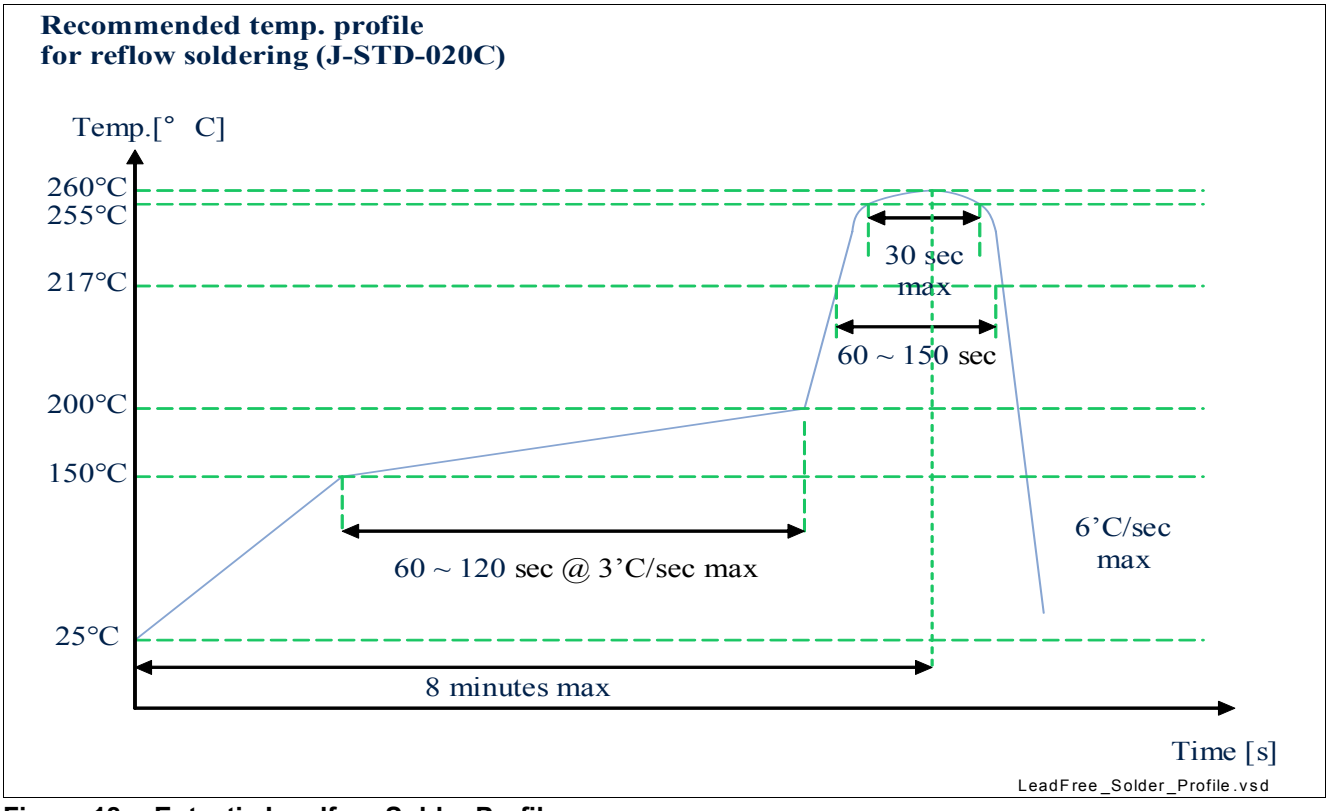

Figure 18 Eutectic Leadfree-Solder Profile

At the reflow process each solder joint has to be exposed to temperatures above solder liquids for a sufficient time to get the optimum solder joint quality, whereas overheating the board with its components has to be avoided. Using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB (especially on large, complex boards with different thermal masses of the components). The most recommended types are therefore forced convection or vapour phase reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary.

The reflow profiles and other reflow parameters are dependent on the used solder paste. The paste manufacturer provides a reflow profile recommendation for this product.

Additionally it is important not to overheat the PAN1322 module by a too large reflow peak temperature. PAN1322 contain several plastic packages and is there by sensitive of the moisture content level at the time of board assembly.

Overheating in combination with excessive moisture content could result in package delaminations or cracks (popcorn effect). The heating rate should not exceed 3°C/s and max sloping rate should not exceed 4°C/s.

PAN1322 shall be handled according to MSL3, which means a floor life of 168h in 30°C/60% r.h.

The PAN1322 module can be soldered according to max. J-STD-020C curve, assuming that all other conditions are followed stated in Product Specification, Qualification Report and in Application Note. Restriction is that PAN1322 can be soldered two times, since one time is already consumed when soldering devices on Module.

10.6 Rework

10.6.1 Removal Procedure

1. Heat the module with an appropriate heating nozzle according to the instruction of the equipment or on a hot plate (about 225°C dependent on the board). Hot plate can only be used if the board is single side assembled. The temperature of the module shall be 200-220°C.
2. Use grippers or a pair of tweezers to remove the module. The module has to be gripped on two opposite edges of the module (not on the shield).
3. Remove excess solder by using solder sucker, suction soldering irons or solder wick.

10.6.2 Replacement Procedure

Replacement can be done in two ways, dependent of how the solder is applied. Solder can be applied either by dispensing on the mother board or by printing the solder paste directly on the module.

10.6.2.1 Alternative 1: Dispensing Solder

A dispenser with controlled volume must be used to assure the same volume on every pad. The volume on each pad shall be about 0.04 mm^3.

1. Dispense 0.04 mm^3 on each LGA pad
2. Pick the module by a nozzle and place in the right position on the board
3. Reflow the solder.

10.6.2.2 Alternative 2: Printing Solder

To print solder on the module a fixture must be used. The purpose of the fixture is to get a flat surface and fix the stencil and module for printing. An example of how this fixture can be designed is shown in **Figure 19**.

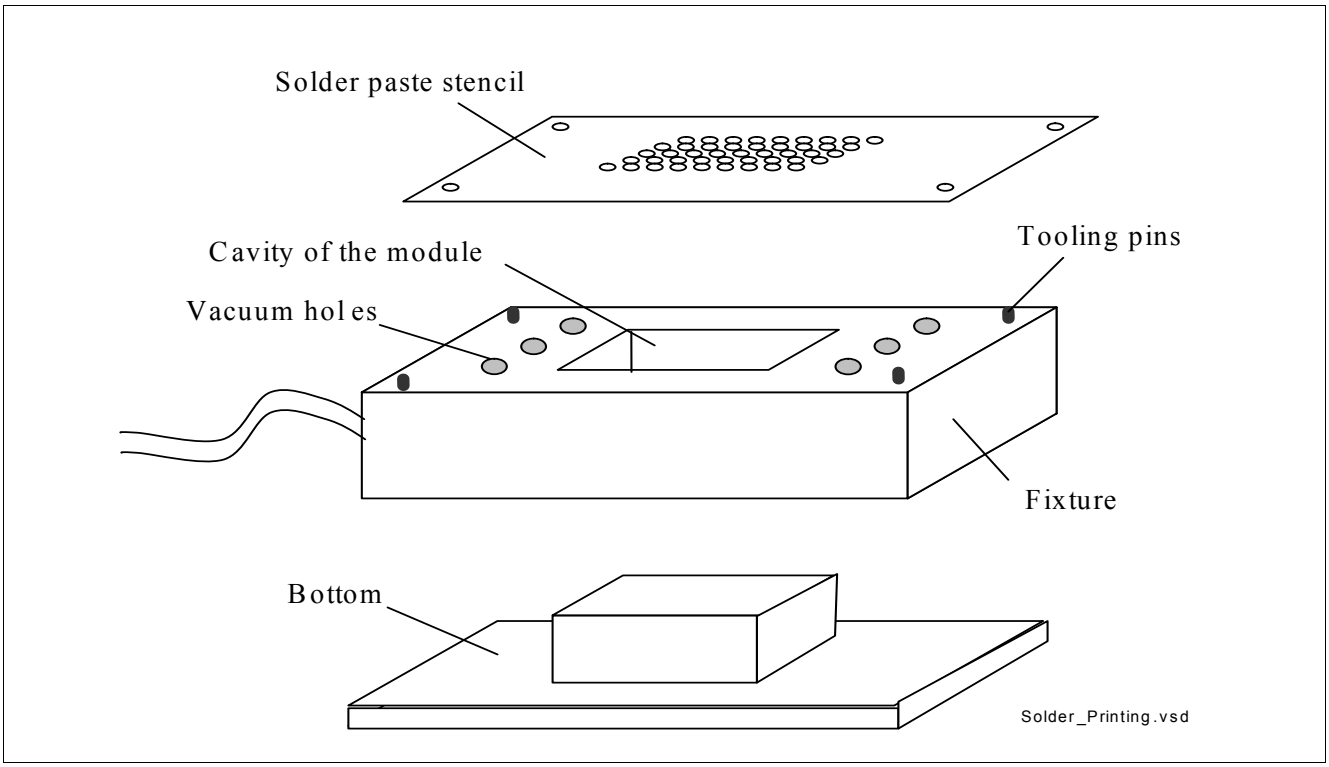

Figure 19 Solder Printing

1. Assemble the fixture to the bottom
2. Place the module in the cavity with the LGA pads upwards
3. Place the solder paste stencil on the fixture and make sure it fits to the tooling pins and the module
4. Apply vacuum to fix the solder paste stencil
5. Apply solder paste on the stencil and print by using a blade
6. Turn everything (bottom, fixture and stencil) upside down.
7. Separate carefully the bottom from the fixture
8. Pick the module by a nozzle and place in the right position on the board
9. Reflow the solder.

10.7 Inspection

Automatic inspection of the solder paste printing before assembly is highly recommended to ensure high yield and good long term reliability.

10.8 Component Salvage

If it is intended to send a defect PAN1322 module back to the supplier for failure analysis, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes ESD precautions, not to apply high mechanical force for component removal, and to prevent excess moisture content in the package during salvage (risk of pop corning failures). Therefore if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried 24h at 125°C before soldering off the defect component, because otherwise too much moisture may have been accumulated.

10.9 Voids in the Solder Joints

10.9.1 Expected Void Content and Reliability

The content of voids is larger on LGA modules than for modules with BGA or leads. At a LGA solder joint the outgassing flux has a longer way to the surface of the solder and it has a relatively small surface to the air.

The void content of the PAN1322 module conforms to IPC-A-610D (25% or less voiding area/area).

Figure 20 shows an example of void-content at a module assembled at production site. Normally you can see the whole spectra of void content variation within the same lot and occasion of assembly.

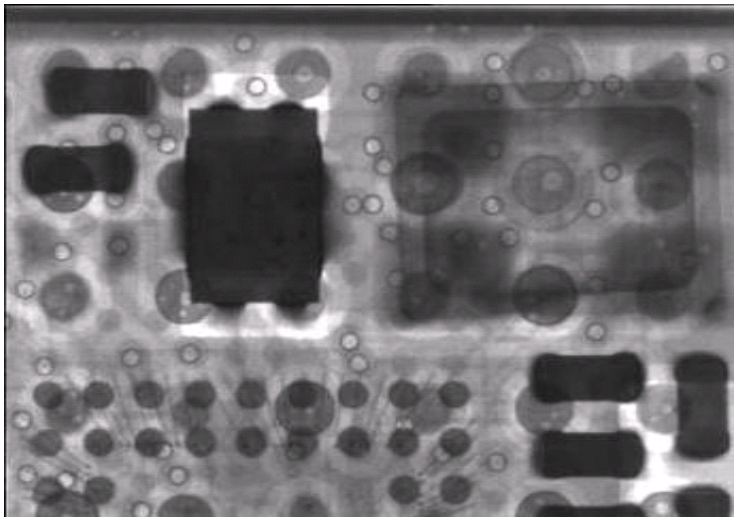

Figure 20 X-ray Picture Showing Voids Conforming to IPC-A-610D

10.9.2 Parameters with an Impact on Voiding

If the void content has to be reduced following parameters have an impact.

Solderability on module and PCB

Bad solderability is often connected to oxidation and has therefore a major impact on voiding. Flux will get entrapped on oxidized surfaces. In general, Ni/Au pads show fewer voids than HASL and OSP.

Solder paste

Higher activity of the flux will remove oxide rapidly and less flux will get entrapped.

Voiding increases with increasing solder paste exposure time, since long exposure time will result in more oxidation and moisture pickup.

Pad size

A large soldering pad means that the outgassing flux has a longer way to the surface of the solder, and will thereby create more voids.

Solder paste

Smaller powder size and higher metal load means more metal surface to deoxidize and thereby more entrapped flux and voiding. Higher metal load does also mean higher viscosity and more difficult for outgassed flux to remove from the solder.

Stencil thickness

A thick solder paste stencil means more surface area to the air and thereby easier for the outgassing flux to leave the solder.

Temperature soldering profile

Too short preheat time means that the flux does not get enough time to react and flux get entrapped in the solder and create voids.

Too long reflow time gives larger voids

Too short reflow time gives a fraction of voids

11 Terminology

A

ACK	Acknowledgement
ACL	Asynchronous Connection-oriented (logical transport)
AFH	Adaptive Frequency Hopping
AHS	Adaptive Hop Sequence
ARQ	Automatic Repeat reQuest

B

b	bit/bits (e.g. kb/s)
B	Byte/Bytes (e.g. kB/s)
BALUN	BALanced UNbalanced
BD_ADDR	Bluetooth Device Address
BER	Bit Error Rate
BMU	BlueMoon Universal
BOM	Bill Of Material
BT	Bluetooth
BW	Bandwidth

C

CMOS	Complementary Metal Oxide Semiconductor
COD	Class Of Device
CODEC	COder/DECoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CTS	Clear To Send (UART flow control signal)
CVSD	Continuous Variable Slope Delta (modulation)
CDCT	Clock Drift Compensation Task
CQDDR	Channel Quality Driven Data Rate

D

DC	Direct Current
DDC	Device Data Control
DM	Data Medium-Rate (packet type)
DMA	Direct Memory Access
DH	Data High-Rate (packet type)
DPSK	Differential Phase Shift Keying (modulation)
DQPSK	Differential Quaternary Phase Shift Keying (modulation)
DSP	Digital Signal Processor
DUT	Device Under Test

E

EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended Synchronous Connection-Oriented (logical transport)
EV	Extended Voice (packet type)

F

FEC	Forward Error Correction
FHS	Frequency Hop Synchronization (packet)
FIFO	First In First Out (buffer)
FM	Frequency Modulation
FW	Firmware

G

GFSK	Gaussian Frequency Shift Keying (modulation)
GPIO	General Purpose Input/Output
GSM	Global System for Mobile communication

H

HCI	Host Controller Interface
HCI+	Infineon Specific HCI command set
HEC	Header Error Check
HV	High quality Voice (packet type)
HW	Hardware

I

I2C	Inter-IC Control (bus)
I2S	Inter-IC Sound (bus)
IAC	Inquiry Access Code
ID	IDentifier
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial Scientific & Medical (frequency band)

J

JTAG	Joint Test Action Group

L

LAN	Local Area Network
LAP	Lower Address Part
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LO	Local Oscillator
LPM	Low Power Mode(s)
LPO	Low Power Oscillator

LSB	Least Significant Bit/Byte
LT_ADDR	Logical Transport Address
M	
MSB	Most Significant Bit/Byte
MSRS	Master-Slave Role Switch
N	
NC	No Connection
NOP	No OPeration
NVM	Non-Volatile Memory
O	
OCF	Opcode Command Field
OGF	Opcode Group Field
P	
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PDU	Protocol Data Unit
PER	Packet Error Rate
PIN	Personal Identification Number
PLC	Packet Loss Concealment
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-On Reset
PTA	Packet Traffic Arbitration
PTT	Packet Type Table
Q	
QoS	Quality Of Service
R	
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send (UART flow control signal)
RX	Receive
RXD	Receive Data (UART signal)
S	
SCO	Synchronous Connection-Oriented (logical transport)
SIG	Special Interest Group (Bluetooth SIG)
SW	Software
SYRI	Synthesizer Reference Input

T

TBD	To Be Determined
TCK	Test Clock (JTAG signal)
TDI	Test Data In (JTAG signal)
TDO	Test Data Out (JTAG signal)
TL	Transport Layer
TMS	Test Mode Select (JTAG signal)
TX	Transmit
TXD	Transmit Data (UART signal)

U

UART	Universal Asynchronous Receiver & Transmitter
ULPM	Ultra Low Power Mode

V

VCO	Voltage Controlled Oscillator

W

WLAN	Wireless LAN (Local Area Network)

12 References

[1] Intel AT Command Specification
(eUniStone_1.00_UM_SD.pdf)
Always the latest revisionwill be available under the link below
(SPP-AT User's Manual)

[2] Release Notes for SPP AT application Software (SW)
(eUniStone_1.00_SW_3.1_RN.pdf)
Always the latest revision will be available under the link below, please refer also to **Table 2 "Firmware Releases as of 2013-05-14" on Page 14**.
(SPP-AT Release Notes)

[3] PAN1322 Application Note Design Guide
Always the latest revision, as a pdf file, will be available under the link below
(PAN1322 Application Note Design Guide)

[4] PAN1322-SPP User's Manual (Data Sheet)
It is this document.
Always the latest revision, as a pdf file, will be available under the link below
(PAN1322-SPP Data Sheet)

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